IN THE CLAIMS

1. (Original) A signal processor system comprising

a power estimation signal,

a variable attack and release stage for detecting changes in amplitude of the power estimation signal relative to time,

comparing the changes in amplitude relative to time to a first criteria,

applying a first algorithm if the change in amplitude does not meet the first criteria,

applying a second algorithm if the change in amplitude does meet the first criteria.

2. (Original) The signal processor of claim 1 wherein the first algorithm includes a factor representing the amount of compression in the system.

3. (Original) The signal processor of claim 1 wherein the first algorithm includes a factor representing the amount of expansion in the system.

4. (Original) The signal processor of claim 1 wherein the first algorithm includes a factor representing user preference.

5. (Original) The signal processor of claim 1 wherein the detected change in amplitude is positive.

6. (Original) The signal processor of claim 1 wherein the detected change in amplitude is negative.

7. (Previously presented) The signal processor of claim 5 wherein the first algorithm includes a first factor representing the amount of compression or expansion in the system.

8. (Original) The signal processor of claim 7 wherein the first algorithm includes a second factor representing user preference.

9. (Canceled)

10. (Original) The signal processor of claim 9 wherein the second algorithm includes a first factor representing the amount of compression or expansion in the system.

11. (Original) The signal processor of claim 10 wherein the second algorithm includes a second factor representing user preference.

12. (Original) The signal processor system of claim 1 wherein the power estimation signal comprises a plurality of power estimation signals.

13. (Original) A variable attack and release processor having an output comprising

an input signal,

a feedback signal,

a comparison stage for providing as a comparison signal a comparison of the input signal and the feedback signal, and

a first stage for applying, in accordance with a first characteristic of the comparison signal, a first algorithm, and providing a first stage output signal in accordance therewith.

14. (Original) The variable attack and release processor of claim 13 further comprising

a second stage for modifying the first algorithm in accordance with at least one of a plurality of secondary characteristics, selected from a group comprising at least one of system parameter signals, user preference signals, feedback signal, and a characteristic of the input signal, a second plurality of algorithms.

15. (Original) The variable attack and release processor of claim 14 wherein the first algorithm includes a plurality of elements in a lookup table.

16. (Original) The variable attack and release processor of claim 15 wherein the second stage modifies the first algorithm by causing the selection of different entries in the lookup table.

17. (Original) The variable attack and release processor of claim 14 wherein the first algorithm is generated by combinatorial logic.

18. (Previously presented) The variable attack and release processor of claim 14 wherein the first algorithm comprises a series of computer programming steps.

19. (Original) The variable attack and release processor of claim 18 wherein the algorithm values are directly calculated.

20. (Original) The processor of claim 13 wherein the first characteristic is a deviation signal between the current input and the current output.

21. (Original) The processor of claim 13 wherein the first characteristic is one of a group of logic states comprising attack, release, and a transition between the two.

22. (Original) The processor of claim 13 wherein the first plurality of algorithms includes filters, linear and non-linear integrators, and time delays.

23. (Original) The processor of claim 14 wherein the first stage output signal comprises a plurality of processed deviation signals.

24. (Original) The processor of claim 13 wherein the input signal includes a plurality of incoming signals.

25. (Original) The processor of claim 13 wherein the feedback signal includes a plurality of feedback signals.

26. (Original) The processor of claim 13 wherein the comparison stage includes a plurality of comparison sub-stages.

27. (Original) The processor of claim 13 wherein the first stage includes a plurality of first sub-stages.

28. (Original) The processor of claim 26 wherein the first stage includes a plurality of first sub-stages.

29. (Original) The processor of claim 13 wherein the first stage output signal comprises a plurality of coefficients.

30. (Original) The processor of claim 14 wherein the first stage output signal comprises a plurality of coefficients resulting from the first stage as modified by the second stage.

31. (Original) The processor of claim 13 wherein the comparison stage further outputs at least one variable.

32. (Original) The processor of claim 31 wherein the comparison stage further outputs a plurality of control variables.

33. (Original) The processor of claim 31 wherein the control variables and coefficients are processed in at least one transform stage in a predetermined manner.

34. (Original) The processor of claim 33 wherein the transform stage implements at least one polynomial equation.

35. (Original) The processor of claim 33 wherein the transform stage processes the control variables and coefficients in accordance with at least one further lookup table.

36. (Original) The processor of claim 33 wherein the transform stage comprises a plurality of sub-transform stages.

37. (Original) The processor of claim 36 wherein each of the plurality of sub-transform stages implements a polynomial.

38. (Original) The processor of claim 37 where each of the polynomials is unique.

39. (Original) The processor of claim 36 further comprising

a combiner stage for combining outputs from at least two of the sub-transform stages.

40. (Original) The processor of claim 13 further including a tracking filter responsive to the first stage output signal and having an output.

41. (Original) The processor of claim 33 further including a tracking filter responsive to the output of the transform stage.

42. (Original) The processor of claim 39 further including a tracking filter responsive to the output of the transform stage.

43. (Original) The processor of claim 33 wherein the output of the tracking filter is a combination of the input signal and the feedback signal.

44. (Original) The processor of claim 33 wherein the output of the tracking filter is representative of a power estimate.

45. (Previously Presented) The processor of claim 44 wherein the power estimate is an intermediate power estimate.

46. (Original) A variable attack and release processor having an output comprising an input signal,

a feedback signal,

a comparison stage for providing as a comparison signal a comparison of the input signal and the feedback signal, and

a tracking filter responsive to an output of the comparison stage for producing an output in accordance therewith.

47. (Original) The variable attack and release processor of claim 46 wherein the output of the tracking filter is a combination of the input signal and the feedback signal.

48. (Original) The variable attack and release processor of claim 46 wherein the output of the tracking filter is representative of a power estimate.

49. (Original) The variable attack and release processor of claim 48 wherein the power estimate signal is an intermediate power estimate.

50. (Original) The variable attack and release processor of claim 46 wherein the comparison signal is a variable.

51. (Original) The variable attack and release processor of claim 46 wherein the comparison signal is a logic signal.

52. (Original) The variable attack and release processor of claim 50 wherein a transform stage receives the comparison signal and provides a transform signal to the tracking filter.

53. (Original) The variable attack and release processor of claim 51 wherein a first stage receives the comparison signal and provides a first stage output to the tracking filter.

54. (Original) The variable attack and release processor of claim 46 wherein the comparison signal comprises both a variable and a logic signal.

55. (Original) The variable attack and release processor of claim 54 wherein a first stage receives the logic signal and provides a first stage output, and the transform stage receives the variable and the first stage output and provides a transform signal to the tracking filter.

56. (Original) The processor of claim 40 wherein the tracking filter comprises a plurality of tracking filters.

57. (Original) The processor of claim 41 wherein the tracking filter comprises a plurality of tracking filters.

58. (Original) The variable attack and release processor of claim 46 wherein the tracking filter comprises a plurality of tracking filters.

59. (Original) The variable attack and release processor of claim 53 further including a second stage responsive to at least one of a group comprising system parameter signal, user preference signal, feedback signal, and a characteristic of the input signal, for modifying the first stage output.

60. (Original) The variable attack and release processor of claim 55 further including a second stage responsive to at least one of a group comprising system parameter signal, user preference signal, feedback signal, and a characteristic of the input signal, for modifying the first stage output.

61. (Original) A signal processor comprising

a power estimation signal

a variable attack and release stage for detecting changes in amplitude of the power estimation signal relative to time,

comparing the changes in amplitude relative to time to a first predetermined threshold,

applying a first correction factor if the change in amplitude does not exceed the first predetermined threshold,

applying a second correction factor if the change in amplitude exceeds the first predetermined threshold.

62. (Original) The signal processor system of claim 1 wherein the power estimation signal is a noise signal.

63. (Original) The variable attack and release processor of claim 13 wherein the input signal is a noise signal.

64. (Original) The variable attack and release processor of claim 46 wherein the input signal is a noise signal.